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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/762,233	02/05/2001	Vitaly A Volodin	Q62631	1665

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2677	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/762,233	VOLODIN, VITALY A	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004 and 20 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *3,5-14 and 16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

In response to the Election of Species Requirement in the Office Action dated April 19, 2004, Applicant elects Species 11, Figures 18 and 19 for examination on which claims 1, 2, 4 and 15 are readable. Applicant reserves the right to file a Divisional Applications directed to the non-elected claims.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of claims 1-2, 4 "applying to the signal electrode, during the selection period, two **additional** (first and second) voltage levels having different polarities with respect to the reference voltage level V0, the same constant modules deviation from the reference voltage level V0 and constant and equal duration the additional the first and second voltage levels being allocated to the boundary portion of the period Tr, so that the first level is allocated to a beginning portion and the second level is allocated to the end portion of period Tr" , limitation of claim 2: "applying to a signal electrode, during a selection period Tr, ... the same constant-modules Vm of deviation from the reference voltage Vo, and constant and equal duration tm/2", limitation of claim 15: "selecting scanning electrodes at least two times a frame in sequence two by two" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-2, 4 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claim limitation of claims 1-2, 4: "applying to the signal electrode, during the selection period, two **additional** (first and second) voltage levels having different polarities with respect to the reference voltage level V0, the same constant modules deviation from the reference voltage level V0 and constant and equal duration the additional the first and second voltage levels being allocated to the boundary portion of the period Tr, so that the first level is allocated to a beginning portion and the second level is allocated to the end portion of period Tr" is not described in specification. In specification description of signified levels Vc (basic levels) was given on page 22, lines 1-5 and page 24, lines 1-5. Claims refer to basic voltages in preceding limitations. Specification is also describes an additional V0-

voltage level having a constant duration is applied to the signal electrode during Tr period (See page 22, lines 5-9). Limitation of claim 15: "selecting scanning electrodes at least two times a frame in sequence two by two" is not described in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 7, 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 7 recite the limitation "**additional** voltages". It is not clear, **additional** to what? To the basic levels, for obtaining current value of brightness, described in the preceding limitations?

Claim 15 recite the limitation: "selecting scanning electrodes at least two times a frame in sequence two by two". It is not clear, what sequence two by two means?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over of Ito et al. (US Patent No. 5,959,603).

As to claim 1, as best understood by examiner, Ito et al. teaches a method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on the other substrate, and liquid crystal cells between electrodes at their intersection points, the cells generating display elements of the display (See Fig. 49, items Y1-Ym, X1-Xn, in description See Col. 1, Lines 25-40), comprising the steps of: selecting scanning electrodes in on group-by-group sequence, applying scanning voltages to selected scanning electrodes, and applying a reference voltage level V0 to the non-selected scanning electrodes (See Figs. 43A-E, items t1,V1, in description See from Col. 1, Line 41 to Col. 2 Line 40); applying to a signal electrode, during selection period, a basic voltage level or levels unequal to or approximately equal to the reference voltage level V0 for obtaining current values of brightness of a selected display element or of a group of selected display elements (See Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67); applying to the signal electrode, during selection period, two voltage levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration (See Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67).

Ito et al. does not show two **additional** levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration to the signal electrode.

It would have been obvious to one of ordinary skill in the art at the time of invention that two additional levels having different polarities, the constant modules of

deviation from V0-level, and constant and equal duration equivalent to the combination of Ito et al. reference level V0 and two signified levels.

As to claim 2, as best understood by examiner, Ito et al. teaches a method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on the other substrate, and liquid crystal cells between electrodes at their intersection points, the cells generating display elements of the display (See Fig. 49, items Y1-Ym, X1-Xn, in description See Col. 1, Lines 25-40), comprising the steps of: selecting scanning electrodes in on group-by-group sequence, applying scanning voltages to selected scanning electrodes, and applying a reference voltage level V0 to the non-selected scanning electrodes (See Figs. 43A-E, items t1,V1, in description See from Col. 1, Line 41 to Col. 2 Line 40); applying to a signal electrode, during selection period Tr, a basic voltage level or levels unequal to or approximately equal to the reference voltage level V0 for obtaining current values of brightness of a selected display element or of a group of selected display elements (See Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67); applying to the signal electrode, during selection period Tr, first and second levels having different polarities with respect to the reference voltage level Vo, the constant modules of deviation from the reference voltage level V0-level, and constant and equal duration tm/2, applying to the signal electrode during selection period Tr after applying the first voltage of a first polarity and before applying the second voltage of a second polarity a third voltage level equal to reference voltage V0 having a constant duration t0 (See Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67).

Ito et al. does not show first and second voltage levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration to the signal electrode.

It would have been obvious to one of ordinary skill in the art at the time of invention that first and second voltage levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration equivalent to the combination of Ito et al. reference level V0 and two signified levels.

5. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over of Ito et al. in view of Admitted Prior Art (APA).

As best understood by examiner, Ito et al. teaches a method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on the other substrate, and liquid crystal cells between electrodes at their intersection points, the cells generating display elements of the display (See Fig. 49, items Y1-Ym, X1-Xn, in description See Col. 1, Lines 25-40), comprising the steps of: selecting scanning electrodes in on group-by-group sequence, applying scanning voltages to selected scanning electrodes, and applying a reference voltage level V0 to the non-selected scanning electrodes (See Figs. 43A-E, items t1,V1, in description See from Col. 1, Line 41 to Col. 2 Line 40); applying to a signal electrode, during selection period, a basic voltage level or levels unequal to or approximately equal to the reference voltage level V0 for obtaining current values of brightness of a selected display element or of a group of selected display elements (See

Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67); applying to the signal electrode, during selection period, two first and second voltage levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration to the signal electrode, the first and second voltage levels being allocated to the boundary portion of the period Tr, so that the first level is allocated to a beginning portion and the second level is allocated to the end portion of the period Tr (See Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67).

Ito et al. does not show two **additional** levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration to the signal electrode.

It would have been obvious to one of ordinary skill in the art at the time of invention that two additional levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration equivalent to the combination of Ito et al. reference level V0 and two signified levels.

Ito et al. does not show applying during the period Tr, voltage levels to the signal electrode in direct or reverse order and alternating, in succeeding periods Tr, the orders of applying of voltage levels to the signal electrode on the basis of changing of the polarity of voltage deviation from the reference voltage V0 in the beginning, in the end of the period Tr, so that the positive polarity is set in the beginning of one period Tr, and the negative polarity is set in the beginning of next period Tr.

APA teaches applying during the period Tr, voltage levels to the signal electrode in direct or reverse order and alternating, in succeeding periods Tr, the orders of

applying of voltage levels to the signal electrode on the basis of changing of the polarity of voltage deviation from the reference voltage V0 in the beginning, in the end of the period Tr, so that the positive polarity is set in the beginning of one period Tr, and the negative polarity is set in the beginning of next period Tr (See Fig. 8, items Tr, Ts).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement timing alternating as shown by APA in the Ito. et al. apparatus in order to reduce DC component and flickering.

6. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. in view of APA and Kobayashi et al . (US Patent No. 5,162,932).

Ito et al. teaches a method of driving a display having a panel including substrates having an array of scanning electrodes on one of substrate, an array of signal electrodes on the other substrate, and liquid crystal cells between electrodes at their intersection points, the cells generating display elements of the display (See Fig. 49, items Y1-Ym, X1-Xn, in description See Col. 1, Lines 25-40), comprising the steps of: selecting scanning electrodes in on group-by-group sequence, applying scanning voltages to selected scanning electrodes, and applying a reference voltage level V0 to the non-selected scanning electrodes (See Figs. 43A-E, items t1,V1, in description See from Col. 1, Line 41 to Col. 2 Line 40); applying to a signal electrode, during a selection period Tr, a basic voltage level or levels unequal to or approximately equal to the reference voltage level V0 for obtaining current values of brightness of a selected display element or of a group of selected display elements (See Fig. 48 B, items Yc, Yd,

in description See Col. 4, Lines 58-67); applying to the signal electrode, during selection period, additional first and second voltage levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration to the signal electrode, the first and second voltage levels being allocated to the boundary portion of the period Tr, so that the first level is allocated to a beginning portion and the second level is allocated to the end portion of the period Tr (See Fig. 48 B, items Yc, Yd, in description See Col. 4, Lines 58-67).

Ito et al. does not show two **additional** levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration to the signal electrode.

It would have been obvious to one of ordinary skill in the art at the time of invention that two additional levels having different polarities, the constant modules of deviation from V0-level, and constant and equal duration equivalent to the combination of Ito et al. reference level V0 and two signified levels.

Ito et al. does not show applying during the period Tr, voltage levels to the signal electrode in direct or reverse order so that the order of their applying to the signal electrode is alternated in succeeding periods Tr.

APA teaches applying during the period Tr, voltage levels to the signal electrode in direct or reverse order and alternating, in succeeding periods Tr, the orders of applying of voltage levels to the signal electrode on the basis of changing of the polarity of voltage deviation from the reference voltage V0 in the beginning, in the end of the

period Tr, so that the positive polarity is set in the beginning of one period Tr, and the negative polarity is set in the beginning of next period Tr (See Fig. 8, items Tr, Ts).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement timing alternating as shown by APA in the Ito. et al. apparatus in order to reduce DC component and flickering.

Ito et al. and APA do not show splitting the voltage pulses applied to signal electrodes into a number of groups being related to different electrodes and shifting the pulses in time concerning their nominal positions in the period Tr so that the values of shifting time are the same for the pulses of single group, but are different for pulses of different groups, and constant for certain period, after termination the time period, other values of shifting time are set in certain or in all groups of voltage pulses or other aggregate of groups of voltage pulses is formed with different values of shifting time in various groups, and the other values of shifting time are set constant for the next time period, after termination of which the process of either changing or setting constant values of shifting are continued providing zero average deviation of duration of duration of each additional level from its nominal duration.

Kobayashi et al. teaches shifting the pulses in time concerning their nominal positions in the period Tr so that the values of shifting time are the same for the pulses of single group, but are different for pulses of different groups, and constant for certain period, after termination the time period, other values of shifting time are set in certain or in all groups of voltage pulses or other aggregate of groups of voltage pulses is formed with different values of shifting time in various groups, and the other values of

shifting time are set constant for the next time period (See Fig. 8, items T1, T2, Tl, Th, Tt, in description See Col. 5, Lines 10-63).

It would have been obvious to one of ordinary skill in the art at the time of invention to shifting the pulses in time concerning their nominal positions in the period Tr so that the values of shifting time are the same for the pulses of single group, but are different for pulses of different groups, and constant for certain period, after termination the time period, other values of shifting time are set in certain or in all groups of voltage pulses or other aggregate of groups of voltage pulses is formed with different values of shifting time in various groups, and the other values of shifting time are set constant for the next time period as shown by Kobayashi et al. in Ito et al. and the APA method in order to provide a driving method for a liquid crystal panel having reduced crosstalk (See Col. 11, Lines 57-58 in the Ito et al. reference) and a reduced number of column voltage levels (See Col. 11, Lines 49-50 in the Ito et al. reference).

Response to Amendment

7. Applicant's arguments filed on 02.10.04 with respect to claims 1-2, 4 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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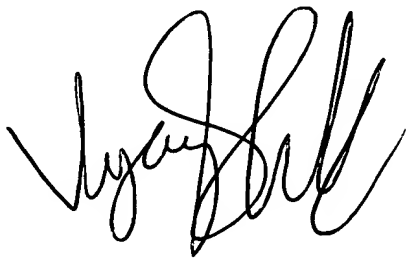

VIJAY SHANKAR
PRIMARY EXAMINER